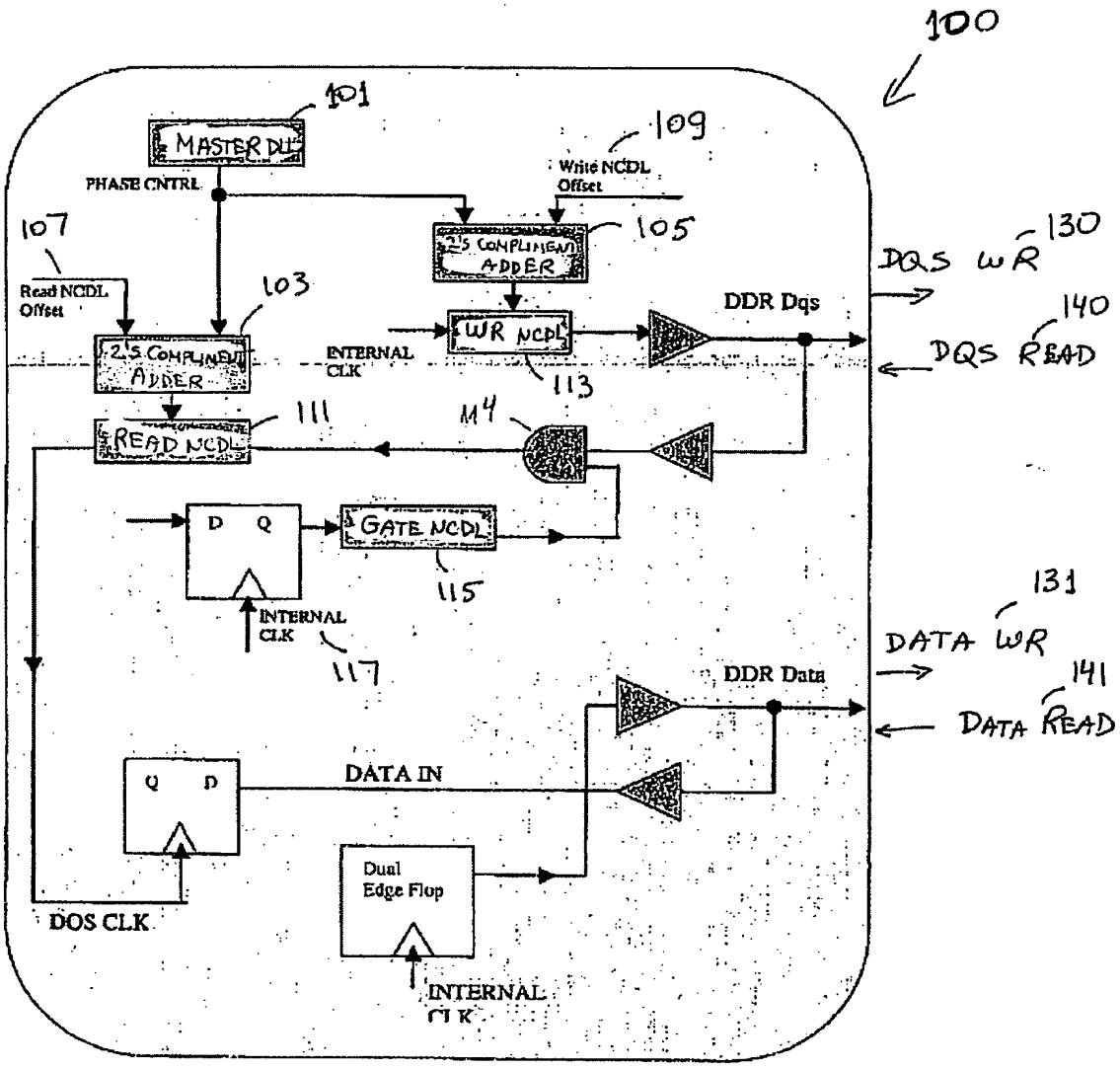

FIG 1A DLL and NCDL mechanism in DDR memory controller

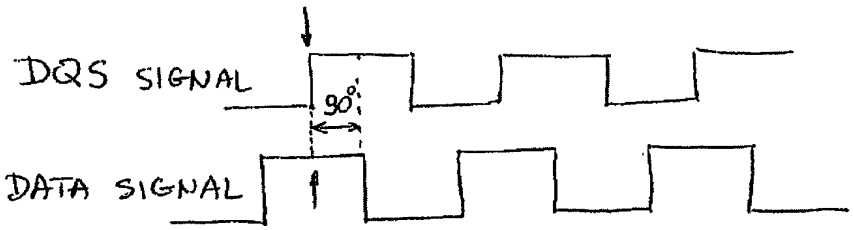

FIG. 1B: CENTER ALIGNMENT OF DQS AND DATA SIGNALS

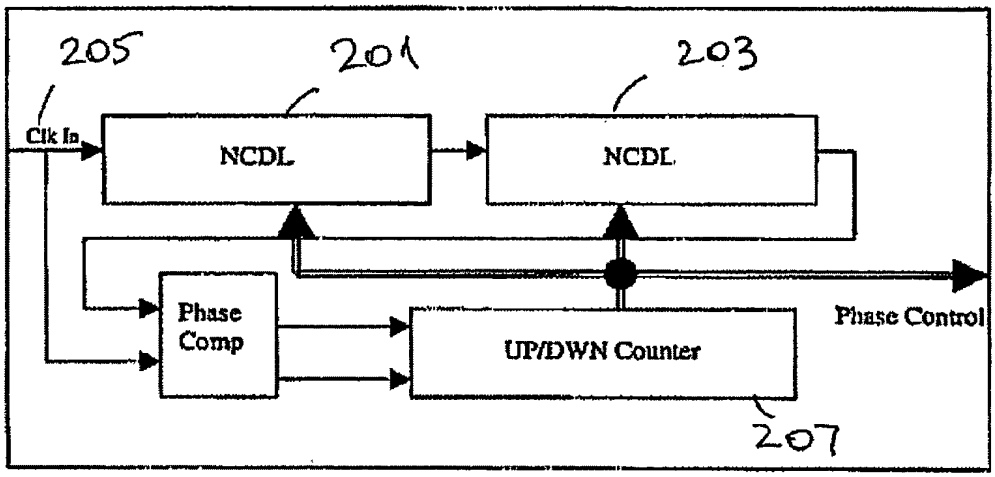

FIG 2: **Delay Locked Loop**

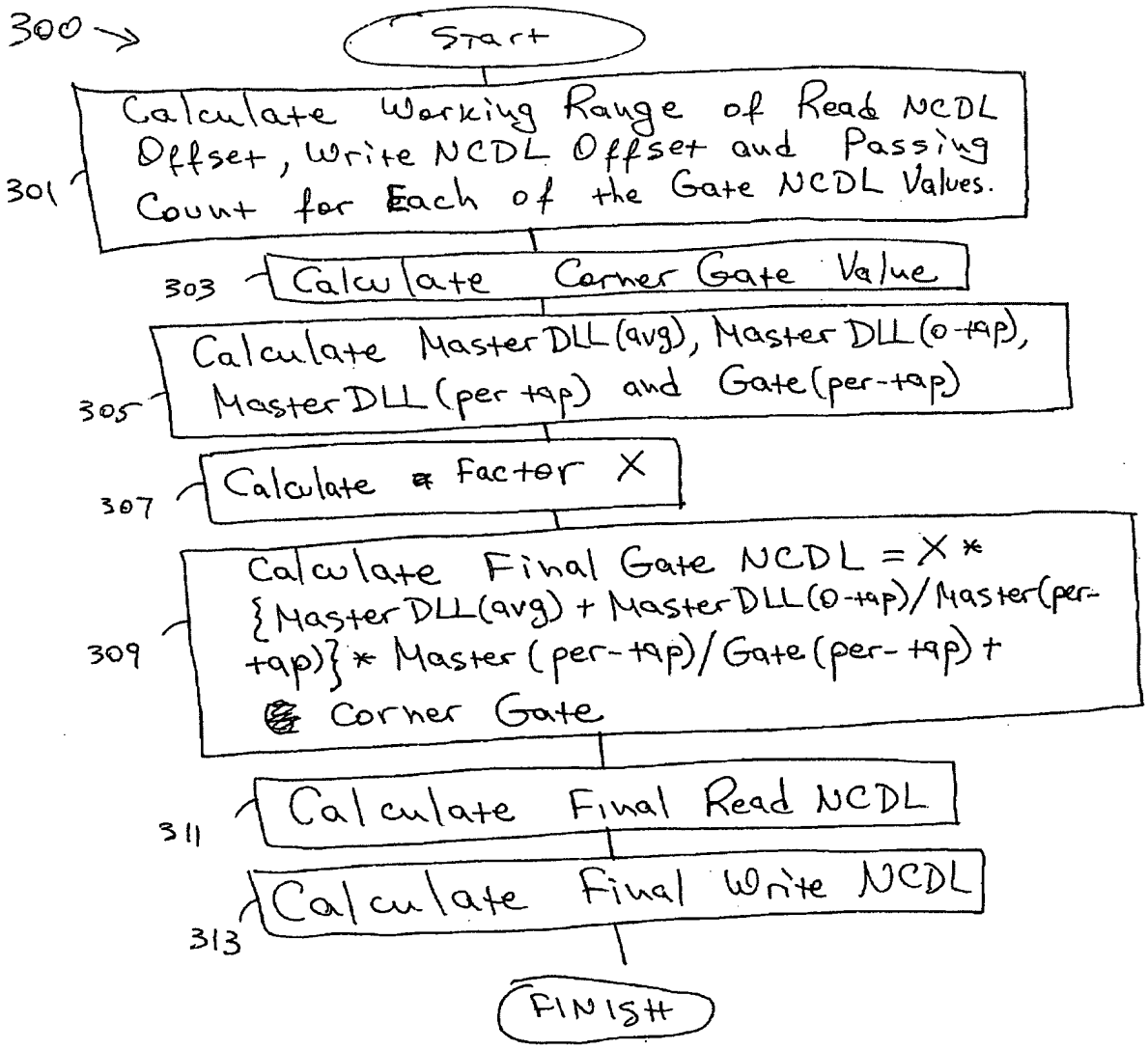
300
Start
Calculate Working Range of Read NCDL Offset, Write NCDL Offset and Passing Count for Each of the Gate NCDL Values.
301
303
Calculate Corner Gate Value
Calculate MasterDLL(avg), MasterDLL(0-tap), MasterDLL(per tap) and Gate(per-tap)
305
Calculate a Factor X
307
Calculate Final Gate NCDL = X * {MasterDLL(avg) + MasterDLL(0-tap)/Master(per-tap)} * Master(per-tap)/Gate(per-tap) + Corner Gate
309
Calculate Final Read NCDL
311
Calculate Final Write NCDL
313
FINISH

FIG. 3

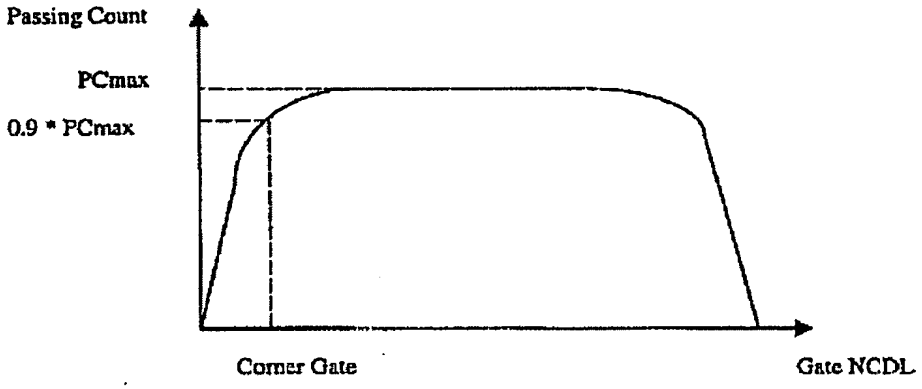

FIG.4: **Plot of Passing Count Vs Gate NCDL**

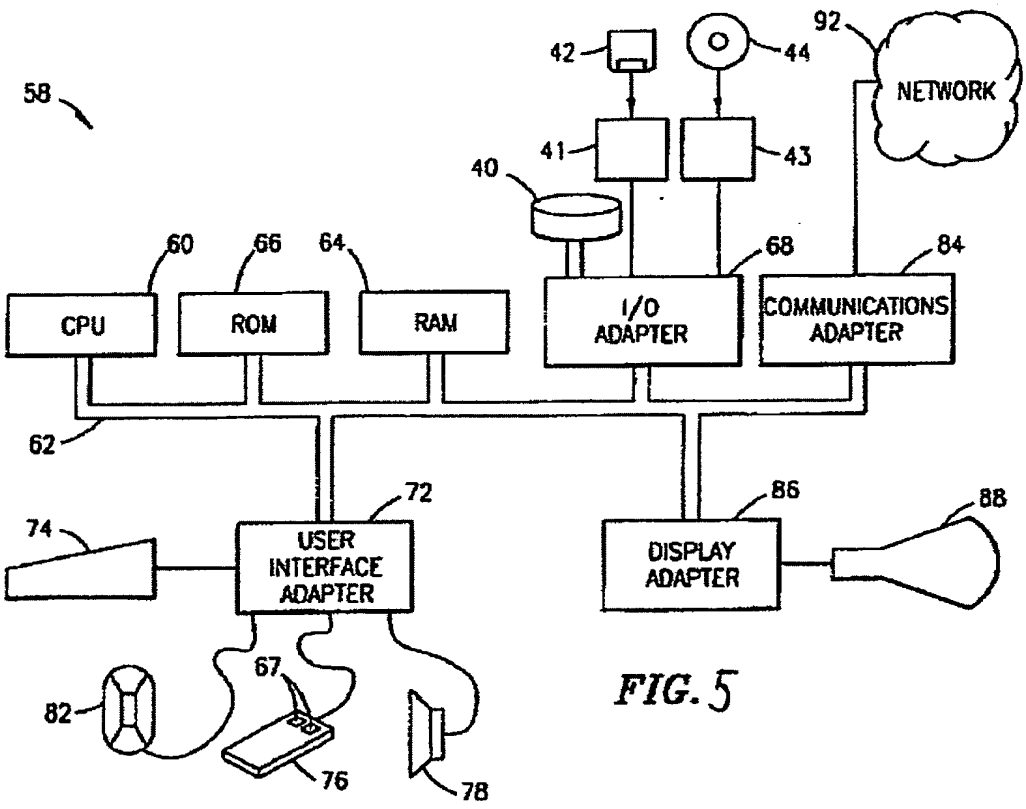
58
42
44
92
NETWORK
41
43
40
60
66
64
68
84
CPU
ROM
RAM
I/O ADAPTER
COMMUNICATIONS ADAPTER
62
72
86
88
74
USER INTERFACE ADAPTER
DISPLAY ADAPTER
67
82
76
78

FIG. 5